APPARATUS AND METHOD FOR RESET DISTRIBUTION

**[0055]** A skew-tolerant, glitch-free reset distribution apparatus and method are provided in an intellectual property (IP) block that supports a multi-channel input/output protocol. During reset mode, synchronizers are used to create more predictable timing, to pipeline the propagation delay, and to tolerate RC-induced skews of up to a clock period in routing a reset signal to all the channels and within the channels in an IP block. Two control signals, which are available from programmable logic resource core circuitry, are used to control the input of the reset signal into the IP block. Because the control signals are designed to be glitch-free, the reset signal is therefore also glitch-free, thus preventing the IP block from inadvertently transitioning into or out of reset mode.